M. TECH. ICT
(Specialization in VLSI Design)

Course Structure and Detailed Syllabus

SCHOOL OF INFORMATION AND COMMUNICATION TECHNOLOGY
GAUTAM BUDDHA UNIVERSITY
GREATER NOIDA – 210308
(INDIA)
### SEMESTER I

<table>
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<tr>
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#### Elective-I

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### SEMESTER – III

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<td>EC673</td>
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Grand Total Credits = 90
SEMESTER I

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UNIT I: Introduction
Digital number systems and information representation; arithmetic operations, decimal and alphanumeric codes, Binary logic, Boolean algebra (identities, functions and manipulation), standard forms, simplification, Logic gates, switch-level and logic CMOS implementation, integrated circuits.

UNIT II: Combinational Logic Design
Components of Combinational Design, Multiplexer and Decoder, Multiplexer Based Design of Combinational Circuits, Implementation of Full Adder using Multiplexer and Decoder, Types of PLD, Combinational Logic Examples, PROM - Fixed AND Array and Programmable OR Array Implementation of Functions using PROM, PLA, PAL, Comparison of PROM, PLA and PAL Implementation of a Function using PAL, Types of PAL Outputs, Device Examples

UNIT III: Sequential Logic Design
Introduction to Sequential Circuits, R-S Latch and Clocked R-S Latch, D Flip Flop, J-K Flip Flop, Master Slave Operation, Edge Triggered Operation, Clocking of Flip-flops, Setup and Hold Times, Moore Circuit, Mealy Circuit Clocking Rules, Sequential Circuits – Design Rules, Sequential Circuit Design Basics, Design of a 4-bit Full Adder using D Flip-flop, Pattern Identifier, State Graph, Transition Table, Implementation of Pattern Identifier, MUX Based Realization, ROM Realization, PAL Implementation

UNIT IV: SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES
PLD families, ROMs, Logic array (PLA), Programmable array logic, GAL, bipolar PLA, NMOS PLA, PAL 14L4, Xilinx logic cell array, I/O Block, Programmable interconnect, Xilinx – 3000 series and 4000 series FPGAs, Altera CPLDs, Altera FLEX 10K series PLDs, Designing a synchronous sequential circuit using PLA/PAL, Realization of finite state machine using PLD

UNIT V: System Design using HDL
HDL operators, Arrays, concurrent and sequential statements, packages, Data flow, Behavioral – structural modeling, compilation and simulation of HDL code, Test bench, Realization of combinational and sequential circuits using HDL, Registers, counters, sequential machine, serial adder, Multiplier-Divider, System Design examples

Text Books:

References:
UNIT I
Introduction to parallel processing: parallelism in uniprocessor system, basic uniprocessor architecture, parallel processing mechanism, balancing of sub system bandwidth, multiprogramming and time sharing, parallel computer structures, pipeline computers, array computers, multiprocessor systems, dataflow computer concept, architectural classification scheme: multiplicity of instruction-data streams, serial versus parallel processing, parallelism versus pipelining, parallel processing applications, productive modeling simulation, engineering design and automation.

UNIT II
Principles of pipelining and vector processing: pipelining- an overlapped parallelism, principles of linear pipelining, clock period, efficiency, throughput, classification of pipeline processors, general pipeline and reservation tables.

UNIT III
Principles of designing pipeline processors: effect of branching, data buffering and bussing structures, internal forwarding and register tagging, hazard detection and resolution, job sequencing and collision prevention, reservation and latency analysis, collision free scheduling, state diagram, greedy cycle, pipeline schedule optimization, pipeline throughput, pipeline efficiency.

UNIT IV
Structure and algorithm for array processors: SIMD array processor, SIMD computer organization, inter – PE communication, SIMD interconnection network, static versus dynamic networks, cube interconnection network, shuffle-exchange omega networks, parallel algorithms and SIMD matrix multiplication.

UNIT V
Multiprocessor architecture and scheduling: functional structure, loosely coupled and tightly coupled multiprocessor, deterministic scheduling strategy, deterministic scheduling model, control flow versus data flow computer, data flow graphs and languages.

References Books:
[9] Quinn, “Parallel Programming in C with MPI and Open MP”, TMH.
UNIT I

UNIT II
Pulse Code Modulation Digital Signal: Quantization, Quantization Error, Pulse Code Modulation (PCM), Signal-to-Noise Ratio in PCM, Companding, Data Rate and Bandwidth of Multiplexed PCM Signal, Inter-symbol Interference, Eye Diagram, Line Coding NRZ, RZ, Biphasic, Duo Binary Etc, Differential PCM (DPCM), Delta Modulation (DM), and Adaptive Delta Modulation (ADM), Slope Overload Error, Granular Noise, Comparison of various systems in terms of Bandwidth and SNR.

UNIT III
Digital Modulation Techniques: Analysis, Generation and Detection (Block Diagram), Spectrum and Bandwidth of Amplitude Shift Keying (ASK), Binary Phase Shift Keying (BPSK), Differential Phase Shift Keying (DPSK), Offset and Non-offset Quadrature Phase Shift Keying (QPSK), M-ary PSK, Binary Frequency Shift Keying (BFSK), M-ary FSK, Minimum Shift Keying, Quadrature Amplitude Modulation (QAM), Comparison of digital modulation techniques on the basis of probability of error, Matched Filter.

UNIT IV

UNIT V

Text Books:

References:
[1] Taub & Schilling, Principles of Communication system, TMH.
# RESEARCH TECHNIQUES IN ICT

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## Unit I: Introduction to Research Techniques
Meaning of research, objectives of research, motivation in research, types of research-Introduction to experimental test bed, algorithmic research, simulation research, mathematical modeling approach, characteristics and prerequisites of research, significance of research, research process, Sources of research problem, criteria of identifying the problem, necessity of defining the problem, errors in selecting research problem, technique involved in defining the problem, Report and paper writing

## Unit II: Data Analysis and Statistical Techniques
Data and their analyses, quantitative methods and techniques, Measure of central tendency, measures of variation, frequency distribution, analysis of variance methods, identifying the distribution with data, parameter estimation, Goodness-of-Fit tests-Chi-Square test, K-S Goodness-of-Fit test, Correlation analysis, Regression analysis, time series and forecasting, Introduction to discriminant analysis, factor analysis, cluster analysis, conjoint analysis. Sampling methods, test of hypothesis.

## Unit III: Random Numbers and Variates
Properties of random numbers, generation, tests for random numbers, random-variate generation Inverse Transform technique, direct transformation, convolution method, acceptance-rejection Technique, Probability distributions functions, Moments, moment generating functions, joint distributions, marginal and conditional distributions, functions of two dimensional random variables Poisson process-Markovian queues, single and multi server models, Little’s formula, steady state analysis

## Unit IV: Algorithmic Research
Algorithmic research problems, types of algorithmic research, types of solution procedure, steps of development of algorithm, steps of algorithmic research, design of experiments,

## Unit V: Simulation and Soft Computing Techniques
Introduction to soft computing, Artificial neural network, Genetic algorithm, Fuzzy logic and their applications, Tools of soft computing, Need for simulation, types of simulation, simulation language, fitting the problem to simulation study, simulation models, verification of simulation models, calibration and validation of models, Output analysis, introduction to MATLAB, NS2, ANSYS, Cadence

### Text Books:

### References:
List of Experiments

1. Introduction to Simulation Software Modelsim.
2. Realization of Gates using VHDL (AND, OR, NOT)
4. Realization of 2 to 4 Decoder using VHDL.
5. Realization of 3 to 8 Encoder using VHDL.
6. Realization of Combinational Design of Multiplexer using VHDL.
7. Realization of Combinational Design of Demultiplexer and Comparator using VHDL.
8. Realization of Functions of Half and Full Adder with different Modeling style using VHDL.
9. Realization of 32 bit ALU using VHDL.
11. Realization of a 4-bit binary, BCD counters and any sequence counter with Synchronous Reset.
12. Realization of a 4-bit binary, BCD counters and any sequence counter with Asynchronous Reset.
13. Realization of VHDL code for 7- Segments Display.
14. Realization of VHDL codes to display messages on given LCD panel.
15. Realization of VHDL code to operate a given stepper motor.
List of Experiments

1. To verify the sampling theorem.

2. To study ASK (Amplitude Shift Keying) System.
   - Modulate a digital signal using amplitude shift keying.
   - Demodulate an amplitude shift keyed signal.

3. To study FSK (Frequency Shift Keying) System.
   - Modulate a digital signal using frequency shift keying.
   - Demodulate a frequency shift keyed signal.

4. To study BFSK (Binary Frequency Shift Keying) System.
   - Modulate a digital signal using Binary Frequency shift keying.
   - Demodulate a Binary Frequency Shift keyed signal.

5. To study PSK (Phase Shift Keying) System.
   - Modulate a digital signal using phase shift keying.
   - Demodulate a phase shift keyed signal.

6. To study BPSK (Binary Phase Shift Keying) System.
   - Modulate a digital signal using binary phase shift keying.
   - Demodulate a binary phase shift keyed signal.

7. To study QPSK (Quadrature Phase Shift Keying) System.
   - Modulate a digital signal using Quadrature phase shift keying.
   - Demodulate a Quadrature phase shift keyed signal.

8. To study DPSK (Differential Phase Shift Keying) System.
   - Modulate a digital signal using differential phase shift keying.
   - Demodulate a differential phase shift keyed signal.

   - Generate, modulate and transmit a pulse coded signal.
   - Receive and demodulate a pulse coded signal.

10. To study TDM (Time Division Multiplexing) System.
    - Generate and transmit a TDM signal.
    - Receive and de-multiplex a TDM signal.

11. To study M-ARY FSK modulation and demodulation.
12. To study and implement the cyclic redundancy check.
13. To study the circuit of PAM modulator and demodulator.
14. To study the circuit of PWM modulator and demodulator.
15. To study the circuit of PPM modulator and demodulator.
SEMESTER II

UNIT I: Crystal Growth, Wafer Preparation, Epitaxy and Oxidation
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II: Lithography and Relative Plasma Etching
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments

UNIT III: Deposition, Diffusion, Ion Implantation and Metallization

UNIT IV: Process Simulation and VLSI Process Integration
Ion implantation, Diffusion and oxidation, Epitaxy, Lithography, Etching and Deposition, NMOS IC Technology, CMOS IC Technology, Memory IC technology, Bipolar IC Technology, IC Fabrication.

UNIT V: Assembly Techniques and packaging of VLSI Devices

Text Books:

References:
UNIT I: Basics in Analog ICs
Analog IC system, Op-Amps, phasors and impedance, Power supply, Transfer functions, filters, bode plots, Integrated circuits, Power speed and efficiency, MOS: as a switch, I/V characteristic, second order effects, device models, amplification, Amplifier: biasing, distortion, two port model, transfer function, frequency response, Noise in circuits, noise in amplifiers, noise bandwidth, small signal modeling for FETs: CS & CE amplifier.

UNIT II: Single Stage and Multistage IC Amplifier

UNIT III: Current Mirrors and Frequency response
Current Mirrors: MOS transistor, BJT, Buffered, Widlar, Wilson, Cascode, as reference current generation, as bandgap reference, as active load in amplifier. Gilbert Analog amplifier,

Frequency response: LF and HF response, transistor model at high frequency, limitation of CE and CS amplifier at low frequency, miller multiplication, open circuit time constant method, frequency response of multistage amplifier, tuned amplifier, mixers.

UNIT IV: Feedback, Stability and Oscillators
Classical feedback system, general considerations, topologies, voltage amplifier, trans-resistance amplifier, current amplifiers, transconductance amplifiers, loop gain estimation, stability of feedback amplifier, Oscillators: Barkhausen criteria, frequency selective RC oscillators, LC & Crystal oscillators.

UNIT V: Analog ICs Special Circuits
Sample and Hold Circuits, Switch Capacitor circuits, Switched capacitor integrators, switched capacitor filter circuits, Data Converter Fundamentals & Architecture: Ideal D/A & A/D converter, Serial and Flash D/A converters and A/D converters, Medium and High Speed converters, Over-sampling converters, CMOS VCO, Ring oscillators, PLL, Gm-C Circuits, rectifiers, comparator.

Text Books:

References:
UNIT I: MOS Transistor theory
NMOS / PMOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation, mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter.

UNIT II: CMOS Design Rules
Lambda Based Design rules, scaling factor, p well / n well / twin well CMOS process, Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect), Circuit elements, resistor, capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, MOS circuits scaling.

UNIT III: Basics of Digital CMOS Design

UNIT V: Dynamic CMOS and clocking
Introduction, advantages of CMOS over NMOS, CMOS/SOS technology, CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing. Clocking-clock generation, clock distribution, clocked storage elements.

UNIT IV: VLSI System Components Circuits and System Level Physical Design
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers, Physical design Delay modeling, cross talk, floor planning, power distribution, Clock distribution.

Text Books:

References:
1. Introduction to Linux OS

2. Introduction to Virtuoso tool and Full Custom IC Design cycle.

3. Realization of an Inverter – I

4. Realization of an Inverter – II

5. Realization of an Inverter – III

6. Realization of an Inverter – IV


11. Realization of Operational Amplifier – II.

12. Realization of Basic DAC Circuit.

13. Realization of R-2R DAC.

14. Realization of Basic ADC Circuit.

15. Realization of SAR based ADC.
ELECTIVE I

Unit I: The Well
Substrate, Parasitic Diode, N-well as a Resistor, N-well patterning and layout, Design Rules, Resistance calculation, N-well Resistor, N-well/Substrate Diode, Carrier Concentrations, Fermi Energy Level, Depletion Layer Capacitance, Storage or Diffusion Capacitance, RC Delay through the N-well, Distributed RC Delay, Distributed RC Rise Time, Twin Well Processes.

Unit II: The Metal Layers

Unit III: The Active and Poly Layers

Unit IV: Resistors, Capacitors, MOSFETs

Unit V: MOSFET Operation
Accumulation, Depletion, Strong Inversion, Threshold Voltage, Characteristics of MOSFETs, MOSFET Operation: Triode and Saturation, Cgs Calculation, Long-Channel MOSFET Models, Model Parameters Related to the Drain Current, Modeling of the Source and Drain Implants Short-Channel MOSFETs Hot Carriers, Lightly Doped Drain, MOSFET Scaling, Short-Channel Effects, Oxide Breakdown, Drain-Induced Barrier Lowering, Gate-Induced Drain Leakage.

Text Books:

References:
UNIT I: RAM Technologies

UNIT II: Non Volatile Memories
Masked Read-Only Memories, High Density ROMs, PROMs, CMOS PROMs, EEPROMs, Floating-Gate EPROM Cell, Electrically Erasable PROMs, EEPROM Technology And Architecture, Nonvolatile SRAM, Flash Memories, Advanced Flash Memory Architecture.

UNIT III: Memory Testing

UNIT IV: Reliability and Radiation Effects

UNIT V: Packaging Technologies

Text Books:
UNIT I: Introduction to RF design and Wireless Technology

UNIT II: RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques, Receiver and Transmitter architectures, Direct conversion and two-step transmitters.

UNIT III: RF Testing
RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

UNIT IV: BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

UNIT V: RF Circuits Design
Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks, Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Mixers- working and implementation. Oscillators- Basic topologies, VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text Book:

References:
Unit I: Introduction
Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

Unit II: Device & Technology Impact on Low Power
Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

Unit III: Low Power Design
Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

Unit IV: Low power Architecture & Systems
Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

Unit V: Power Optimization Techniques
Design time power optimization, circuit level power optimization, various architectural level methods for optimization, estimation and optimization of interconnects parasitic and delays, Low power clocking and system optimization, Standby low power optimization, Run Time voltage optimization and estimation.

Text Books:

References:
MIXED SIGNAL VLSI DESIGN

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**Unit 1: Signals, Filters, and Tools**

Sinusoidal Signals, Pendulum Analogy, Amplitude in the x-y Plane, In-Phase and Quadrature Signals, Complex (z-) Plane, Comb Filters, Digital Comb Filter, Digital Differentiator, Intuitive Discussion of the z-Plane, Comb Filters with Multiple Delay Elements, Digital Integrator, Delaying Integrator, Exponential Fourier Series, Fourier Transform, Dirac Delta Function.

**Unit 2: Sampling and Aliasing**


**Unit 3: Analog Filters**


**Unit 4 Digital Filters**

Models for DACs and ADCs, Ideal DAC, Modeling of Ideal DAC, Ideal ADC, Number Representation, Increasing Word Size, Adding Numbers and Overflow, Two's Complement Sinc-Shaped Digital Filters, Counter, Aliasing, Accumulate-and-Dump, Lowpass Sinc Filters, Averaging without Decimation, Cascading Sinc Filters, Finite and Infinite Impulse Response Filters, Bandpass and Highpass Sinc Filters, Frequency Sampling Filters.

**Unit 5: Data Converter SNR**

Quantization Noise, Quantization Noise Spectrum, Bennett's Criteria, RMS Quantization Noise Voltage, Quantization Noise as a Random Variable, Quantization Noise Voltage Spectral Density, Power Spectral Density, SNR, Effective Number of Bits, Coherent Sampling, SNDR, Spurious Free Dynamic Range, Dynamic Range, Specifying SNR and SNDR, Clock Jitter.

**Text Books:**


**References:**

List of Experiments

1. Introduction to simulation software ANSYS using GUI.
2. Introduction to simulation software ANSYS using Command lines.
3. Simulation and Realization of Capacitive Acceleration Sensor using ANSYS.
4. Modal and harmonic analysis of Silicon Beam Actuator using ANSYS.
5. Multiphysics Analysis of a Thermal Actuator using ANSYS.
6. Simulation and Realization of Axisymmetric model of a piezoresistive pressure sensor.
7. Electromechanical Simulation and Modeling of RF MEMS Capacitance using ANSYS.
9. Reduced Order Modeling of RF MEM Capacitance.
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**ELECTIVE III AND IV**

**UNIT I : Introduction to ASICs, CMOS Logic and ASIC Library Design**
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

**UNIT II: Programmable ASICs, Programmable ASIC Logic Cells and ASICs I/O Cells.**
Anti fuse, static RAM, EPROM and EEPROM technology, PREP benchmarks, Actel ACT, Xilinx LCA, Altera FLEX , Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

**UNIT III: Programmable ASIC Interconnect, Programmable ASIC Design Software and Low Level Design Entry**

**UNIT IV: Logic Synthesis, simulation and Testing**
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation- boundary scan test - fault simulation - automatic test pattern generation.

**UNIT V: ASIC Construction, Floor Planning, Placement and Routing**
System partition, FPGA partitioning, partitioning methods, floor planning, placement, physical design flow, global routing, detailed routing, special routing, circuit extraction, DRC.

**Text Books:**

**References:**
M.Tech ICT                                          VLSI Design
Effective from 2013-14
UNIT I: Introduction to MEMS Technology
Introduction and Origin of MEMS, driving force for MEMS development, Application of MEMS, MEMS fabrication technologies: Conventional IC Vs MEMS fabrication processes, Micromachining Technology and Process, LIGA process, Wafer Bonding, MEMS Packaging

UNIT II: Mechanics for MEMS Design
Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III: MEMS Sensor and Actuation Principles
Sensors, Classification and terminology of Sensors, evolution of Semiconductor sensors, sensor characterization basic concept of acoustic, mechanical, magnetic, thermal sensors and integrated sensors. Actuation of MEMS devices, electrostatic actuation, and parallel plate capacitor- cantilever beam based movement, comb-drive structures.

UNIT IV: Modeling and Realization of RF MEMS components
Typical features of RF and wireless system. The functionality, modeling and implementation issues of central RF MEMS components: Capacitors/ Inductors, Varactor, Switches, RF Power Attenuator, Power Amplifier, Impedance Matching Network, transmission lines, phase shifters, resonators, filters and oscillators, Antenna, different modeling styles in RF MEMS devices.

UNIT V: Packaging, Reliability and Integration of RF MEMS
Overview of packaging, possibilities for monolithic integration of RF MEMS with microelectronics, Reliability issues in RF MEMS, Case studies on more composite RF MEMS systems.

Text Books:

References:
UNIT I: Probability Plotting and Load- Strength Interference
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference, Safety margin and loading roughness on reliability.

UNIT II: Reliability Prediction, Modeling and Design
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, Petri Nets, State space Analysis, Monte Carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III: Electronics and Software System Reliability
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV: Reliability Testing and Analysis
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V Manufacture and Reliability Management
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programs, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

Text Books:

Reference:
**UNIT I: DSP Integrated Circuits and VLSI Circuit Technologies**
Standard digital signal processors, Application specific IC’s for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic.

**UNIT II: Digital Signal Processing**

**UNIT III: Digital Filters and Finite Word length Effects**
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

**UNIT IV DSP Architectures and Synthesis of DSP Architectures**
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. DSP algorithms hardware mapping, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

**UNIT V Arithmetic Units and Integrated Circuit Design**
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

**Text Books:**

**References:**
UNIT I: Introduction

UNIT II: Logic Simulation

UNIT III: Fault Modeling and Simulation

UNIT IV: Testing for Faults

UNIT V: Design for Testability
Testability: Tradeoffs, Controllability and Observability, Ad Hoc Design for Testability Techniques: Test points, Initialization, Monostable multivibrators, Oscillators and Clocks, Controllability and Observability by means of scan registers, Generic scan based designs.

Text Books:

References:
UNIT I: Introduction

UNIT II: Circuit Partitioning and Floorplanning

UNIT III: Placement

UNIT IV: Routing

UNIT V: Advanced Topics

Text Books:

References: